**IN THE CLAIMS:**

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1, 7, 11, and 12, and CANCEL claims 2-6, 10, and 22-47 in accordance with the following:

1. (CURRENTLY AMENDED) An apparatus for controlling an output of a laser diode in an optical medium apparatus, comprising:

a sampling circuit sampling said output of said laser diode at a predetermined frequency according to a write pulse and generating a sampled signal; ~~and~~

an arithmetic unit receiving said sampled signal, generating a control power value applied to the laser diode in response to said sampled signal, and modifying said output of said laser diode in response to said control power value; and

a controller connected to said sampling circuit and said arithmetic unit, said controller including:

a write pulse generator generating power control signals based on a non-return to zero inverted signal and generating a write control signal indicating power applied to said laser diode based on said power control signals; and

a sampling controller connected to said write pulse generator, generating a selection signal, controlling said sampling circuit and said arithmetic unit based on said write control signals generated by said write pulse generator.

2. (CANCELLED)

3. (CANCELLED)

4. (CANCELLED)

5. (CANCELLED)

6. (CANCELLED)

7. (CURRENTLY AMENDED) The apparatus of claim ~~6~~1, further comprising a preprocessor interposed between said current/voltage converter and said analog to digital converter, controlling the gain of said voltage signal output from said current/voltage converter.

8. (ORIGINAL) The apparatus of claim 7, wherein said preprocessor comprises:

a read/write gain controller controlling the gain of said voltage signal output from said current/voltage converter in a read/write operational mode, generating a gain controlled power level signal; and

a gain select switch selecting either one of said voltage signal of said current/voltage converter and said gain controlled power level signal of said read/write gain controller, and generating a gain controlled output signal and providing the selected output to said analog/digital converter].

9. (ORIGINAL) The apparatus of claim 8, wherein said preprocessor comprises:

a low-pass filter filtering said gain controlled output signal of said gain select switch, generating a low-pass filter signal;

a peak holder holding a peak value from said gain controlled output signal of said gain select switch, and generating a peak holding signal;

a bottom holder holding a bottom value from said gain controlled output signal of said gain select switch, and generating a bottom holding signal; and

a mode select switch connected to said gain select switch, said low pass filter, said peak holder, and said bottom holder, selecting one of said gain controlled output signal, said low-pass filter signal, said peak holding signal, and said bottom holding signal, and providing the selected output to the analog/digital converter.

10. (CANCELLED)

11. (CURRENTLY AMENDED) The apparatus of claim ~~10~~1, further comprising a delay delaying said write control signal transmitted from said write pulse generator to said

sampling controller and providing said sampling controller with a delayed write control pulse, and controlling said sampling controller to generate said selection signal in accordance with said delayed write control signal.

12. (CURRENTLY AMENDED) The apparatus of claim ~~10~~1, further comprising:

an interface connected to an external source, receiving interface signals including a clock signal, a read/write control signal, said NRZI signal and a land/groove determination signal; and

an APC controller connected between said interface and said write pulse generator and said sampling controller controlling said write pulse generator and said sampling controller in response to said interface signals.

13. (ORIGINAL) The apparatus of claim 1, wherein said arithmetic unit comprises:

a reference power selector having reference registers storing reference power values, and generating a reference power value so as to control a selected power value of said output of said laser diode;

a control power selector having control registers storing control power values, generating a control power value;

a subtracter connected to said sampling circuit and said reference power selector, measuring a difference between said reference power value and said power values provided by said sampling circuit, generating a difference signal;

an adder connected to said control power selector and said subtractor, adding said difference signal to said control power value, and generating an added signal; and

a demultiplexer connected to said adder, selecting one of said control registers so as to store said added signal in said one of said control registers.

14. (ORIGINAL) The apparatus of claim 13, further comprising a divider connected between said subtracter and said adder, said divider reducing said difference signal by a predetermined amount and providing a reduced difference signal to said adder.

15. (ORIGINAL) The apparatus of claim 13, further comprising an averaging unit averaging said sampled signal of said sampling circuit and providing an average control signal to said subtracter, said subtracter generating said difference signal in response to said average control signal and said reference power value.

16. (ORIGINAL) The apparatus of claim 15, wherein said average power value control signal of said averaging unit is transmitted to a micro processor.

17. (ORIGINAL) The apparatus of claim 13, further comprising:

a controller generating a selection signal;

said reference power selector comprising:

a first multiplexer selecting one of said reference registers, and

a second multiplexer selecting one of said control registers and providing said control power value stored in said one of said control registered to said adder, wherein said first and second multiplexers and said demultiplexer are synchronized by said selection signal generated by said controller.

18. (ORIGINAL) The apparatus of claim 17, further comprising:

a third multiplexer connected to said control registers, selecting one of said control registers according to a write control signal generated from said controller; and

a digital/analog converter connected to said third multiplexer, converting an output of said third multiplexer into an analog signal and providing said analog signal to said laser diode.

19. (ORIGINAL) The apparatus of claim 17. further comprising a data output terminal connected to said control power selector, outputting said selected control power value stored in said selected control register to an outside of said arithmetic unit.

20. (ORIGINAL) The apparatus of claim 17, further comprising a data input terminal connected to said control power selector, said control power value being stored in said selected control register when transmitted to said control power selector through said data input terminal.

21. (ORIGINAL) The apparatus of claim 20, further comprising a fourth multiplexer connected between said adder and said control power selector, generating said control power value in response to one of said reference power value and said added signal, said control power selector storing one of said reference power value and said added signal in one of said control registers.

22-47. (CANCELLED)